

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Kelly T. Hurley

Serial No.:

Filed: February 26, 2004

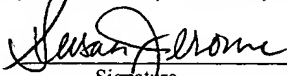
For: OPTIMIZED FLASH MEMORY CELL

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§ Group Art Unit:
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§ Examiner:
§
§ Atty. Docket: 2000-0116.01/US
§
§ Paper No.
§

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

<p align="center">Certificate of Express Mailing (37 CFR § 1.10)</p> <p>"Express Mail" mail label number: <u>ET658403150US</u></p> <p>Date of Deposit: <u>February 25, 2004</u></p> <p>I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p align="right"> Signature</p>
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In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant respectfully requests that this Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R. § 1.97(g), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
6,271,087	08/07/2001	Kinoshita et al.
6,188,115	02/13/2001	Kamitani
6,080,624	06/27/2000	Kamiya et al.
5,994,733	11/30/1999	Nishioka et al.
5,731,242	03/24/1998	Parat et al.
5,210,047	05/11/1993	Woo et al.

Other References

"A 130-mm², 256-Mbit NAND Flash with Shallow Trench Isolation Technology", Kenichi Imamiya et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999

"Novel 0.44μm² Ti-Salicide STI Cell Technology for High Density NOR Flash Memories and High Performance Embedded Application", H. Watanabe et al., IEDM 98, pp. 975-978

As this information is being submitted within three months of the date of filing of the application, Applicant understands that no fee or certification is required for the submission and consideration of this information at this time.

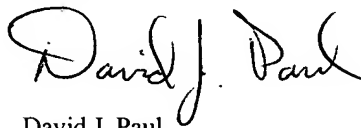
If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned attorney at the number indicated.

* * * *

A Form PTO-1449 is enclosed herewith.

Date: 02/26/2004

Respectfully submitted,



David J. Paul
Reg. No. 34,692
Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83706-9632
(208) 368-4515
AGENT FOR APPLICANT

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 2000-0116.01/US	Serial No:
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))		Applicant: Kelly T. Hurley	
		Filing Date: February 26, 2004	Group:

(use several sheets if necessary)

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	
AA	6,271,087	08/07/2001	Kinoshita et al.	438	258	
AB	6,188,115	02/13/2001	Kamitani	257	412	
AC	6,080,624	06/27/2000	Kamiya et al.	438	257	
AD	5,994,733	11/30/1999	Nishioka et al.	257	316	
AE	5,731,242	03/24/1998	Parat et al.	438	586	
AF	5,210,047	05/11/1993	Woo et al.	437	43	
AG						
AH						
AI						
AJ						
AK						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AL					<input type="checkbox"/>	<input type="checkbox"/>
	AM					<input type="checkbox"/>	<input type="checkbox"/>
	AN					<input type="checkbox"/>	<input type="checkbox"/>
	AO					<input type="checkbox"/>	<input type="checkbox"/>
	AP					<input type="checkbox"/>	<input type="checkbox"/>
	AQ					<input type="checkbox"/>	<input type="checkbox"/>

Initial

OTHER ART (including author, title, date, pertinent pages, etc.)

	AR		"A 130-mm ² , 256-Mbit NAND Flash with Shallow Trench Isolation Technology", Kenichi Imamiya et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 11, November 1999
	AS		"Novel 0.44μm ² Ti-Salicide STI Cell Technology for High Density NOR Flash Memories and High Performance Embedded Application", H. Watanabe et al., IEDM 98, pp. 975-978
	AT		

Examiner:	Date Considered:
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.